Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (canceled)

Claim 5 (currently amended): A semiconductor device, which is formed by combining and disposing pre-registered functional blocks, and determining a wiring pattern in accordance with a given logic circuit specification, wherein:

~~each of~~at least one of the functional blocks has a logic circuit and a diode; and

the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, ~~the diode being connected to an input terminal, which is to be potential-clamped, among input terminals of the functional blocks~~

the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 6 (previously presented): The semiconductor device as claimed in Claim 5, wherein the logic circuit is a memory.

Claim 7 (currently amended): A method of designing a semiconductor device, which is formed by combining and disposing pre-registered functional blocks, and determining a wiring pattern in accordance with a given logic circuit specification, comprising the steps of:

registering the functional blocks in advance,

wherein ~~each of~~at least one of the functional blocks has a logic circuit and a diode, and

wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, ~~the diode being connected to an input terminal, which is to be potential-clamped, among input terminals of the functional blocks~~

the diode is connected to a potential-clamped input terminal of the at least one the functional blocks.

Claim 8 (previously presented): A computer-readable recording medium, on which the method of designing a semiconductor device, as claimed in Claim 7, is stored as a program to be executed by a computer.

Claim 9 (currently amended): A design support apparatus for a semiconductor device, which is formed by combining and disposing pre-registered functional blocks, and determining a wiring pattern in accordance with a given logic circuit specification, comprising:

registration means for registering the functional blocks in advance,

wherein ~~each of~~at least one of the functional blocks has a logic circuit and a diode, and

wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a ~~power source, the diode being connected to an input terminal, which is to be~~ potential-clamped~~, among~~ input terminal[[s]] of the at least one of the functional blocks.

Claim 10 (new): A semiconductor device which is formed by combing and disposing pre-registered functional blocks, and determining a wiring pattern in accordance with a given logic circuit specification, wherein:

at least one of the functional blocks including functional blocks has a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ratio; and

the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source,

the diode is connected a potential-clamped input terminal of the at least one of the functional blocks.

Claim 11 (new): The semiconductor device as claimed in

Claim 10, wherein the logic circuit is a memory.

Claim 12 (new): A method of designing a semiconductor device, which is formed by combining and disposing pre-registered functional blocks, and determining a wiring pattern in accordance with a given logic circuit specification, comprising the steps of:

registering the functional blocks in advance,

wherein at least one of functional blocks has a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ration;

wherein the diode is composed of a first conduction type diffusion later and a second conduction type well connected to a power source,

the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 13 (new): A computer-readable recording medium, on which the method of designing a semiconductor device, as claimed in Claim 12, is stored as a program to be executed by a computer.

Claim 14 (new): A design support apparatus for a semiconductor device, which is formed by combining and disposing pre-registered functional blocks, and determining

a wiring pattern in accordance with a given logic circuit specification, comprising:

registration means for registering the functional blocks in advance,

wherein at least one of the functional blocks has a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ratio, and

wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a potential-clamped input terminal of the at least one of the functional blocks.